Arabian™* Troubleshooting Guide

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4M

ATARI

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Troubleshooting with the Atari CAT Box and Z80 Interface Adapter

Preliminary CAT Box Set-Up

1. Disconnect the electrical power from the game.
2. Disconnect the wiring harness from the game PCB.
3. Remove the game PCB from the game cabinet. Remove the Z80 Microprocessor IC15 from the game PCB.
4. Connect the CAT Box flat cable connector to the 50-pin connector of the CAT Box/Z80 Interface Adapter.
5. Connect one end of the 40-pin flat cable supplied with the Interface Adapter to the 40-pin connector of the Interface Adapter.
6. Connect the other end of the 40-pin flat cable to the socket of Z80 microprocessor IC15 on the game PCB.
7. Connect the DATA PROBE ground of the CAT Box to the ground bus bar adjacent to Game Microprocessor IC15 on the game PCB.
8. Apply power to both the CAT Box and the game.
9. Set the following CAT Box switches as indicated:

   R/$\overline{W}$ MODE: (OFF)
   R/$\overline{W}$: WRITE
   BYTES: 1024
   DBUS SOURCE: ADDR
   TESTER MODE: R/$\overline{W}$
   TESTER SELF-TEST: OFF
10. Press the TESTER RESET button on the CAT Box.

Troubleshooting with the Read/Write Controller

Working RAM (IC10) Check

Check the Working RAM of the game PCB as follows:

1. Perform the preliminary set-up procedure.
2. Enter address D000 on the CAT Box keyboard. Check that D000 is shown on the ADDRESS/SIGNATURE display of the CAT Box.
3. Set R/$\overline{W}$ MODE to PULSE and then back to (OFF).
4. Set R/$\overline{W}$ to READ.
5. Set R/$\overline{W}$ MODE to PULSE.
6. Check the COMPARE ERROR light-emitting diode (LED) on the CAT Box. If this LED is off, the game Working RAM is okay. If this LED is turned on, first check that all interconnections between the CAT Box, Interface Adapter, and game PCB are correctly and securely made. Then repeat parts 1 through 6 of this procedure. If the COMPARE ERROR LED lights up again, check the game Working RAM for failure.

Display RAM (IC154–185) Check

Check the Display RAM of the game PCB as follows:

1. Perform the Preliminary Set-Up Procedure.
2. Perform the Working RAM Check.
3. Set the following CAT Box switches as indicated:

   R/$\overline{W}$: WRITE
   R/$\overline{W}$ MODE: (OFF)
   DBUS SOURCE: DATA
   BYTES: 1
4. Write FF to address E000. To write data from the CAT Box to the game memory, first set R/$\overline{W}$ to WRITE. Then, enter the hexadecimal address with the keyboard on the CAT Box. Check that the address shown in the ADDRESS/SIGNATURE display of the CAT Box is correct. Then press the DATA SET button and enter the hexadecimal data with the keyboard on the CAT Box. Check that the data shown in the DATA display is correct. Then set R/$\overline{W}$ MODE to PULSE and back to (OFF) to send the data to the game memory address shown in the ADDRESS/SIGNATURE display.
5. Write 07 to address C800 and 40 to address CA00. Then write 0E to address C800 and 08 to address CA000.
6. Set BYTES to 1024.
7. Write 00 to addresses 8000, 8400, 8800, 8C00, 9000, 9400, 9800, 9C00, A000, A400, A800, AC00, B000, B400, B800, and BC00.
8. Check that a section of the game display is erased when the R/$\overline{W}$ MODE switch is used to write data to each of the above addresses. The erasing begins at the top of the display and proceeds downward by sections.

Troubleshooting with Checksums

NOTE

The following procedure can only be done with those CAT Boxes equipped with a Checksum Switch.

Program ROM (IC1–4) Check

1. Perform the CAT Box preliminary set-up.
2. Set the CAT Box switches as indicated:

   BYTES: 256
   DBUS SOURCE: DATA
   R/$\overline{W}$ MODE: OFF
   CHECKSUM SWITCH: ON
   R/$\overline{W}$: READ
3. Key in the address pattern given in Table 1 (use *0000* to start).
4. Set the R/$\overline{W}$ MODE switch to PULSE and then back to (OFF).
5. Check the CAT Box ADDRESS/SIGNATURE display for the appropriate checksum.
6. Repeat steps 3 through 5 for each address listed in Table 1.

Table 1 Program ROM Checksums

ADDRESS	ROM TESTED	CHECKSUM
0000	ROM0	29E0
2000	ROM1	8FF8
4000	ROM2	47CA
6000	ROM3	C594

Troubleshooting with Signature Analysis

NOTE

The signatures checked in the following procedure are printed in color on the Game Microprocessor and Address Decoders schematic diagrams shown on Sheet 6A and 6B in the Schematic Package Supplement.

Address Bus Lines and Address Decoders Check

1. Perform the CAT Box preliminary set-up.
2. Connect the three BNC-to-EZ clip cables supplied with the CAT Box to the SIGNATURE ANALYSIS CONTROL START, STOP, and CLOCK jacks of the CAT Box.
3. Connect the three black EZ clips to the ground bus bar adjacent to the Game Microprocessor IC15.
4. Set the CAT Box switches as indicated:

   TESTER MODE: SIG
   TESTER SELF-TEST: OFF
   PULSE MODE: LATCHED
   START: Positive-going edge trigger
   STOP: Positive-going edge trigger
   CLOCK: Positive-going edge trigger
5. Press TESTER RESET on the CAT Box.
6. Connect the CAT Box Signature Analysis probe tips as indicated:

   START: pin 12 of IC16
   STOP: pin 12 of IC16
   CLOCK: pin 14 of IC36
7. Verify the set-up connections by connecting the DATA PROBE to the Game Microprocessor IC15. The CAT Box ADDRESS/SIGNATURE display should show *0000*. Now connect the DATA PROBE to the +5V bus adjacent to the Sound Microprocessor IC27. The ADDRESS/SIGNATURE display should show *00UP*.

NOTE

While testing decoders and ROMs, adding 270 pF capacitors to AB12, A13, A14, and A15 may be necessary to eliminate unstable signatures.

8. Probe the IC pins with the DATA PROBE and check for the signature indicated in color on the Game Microprocessor and Address Decoders schematic diagrams (Sheet 6A and 6B).

Signal Name Descriptions for Arabian

A0–A15
Address bits on Microprocessor Address Bus lines A0–A15 are generated by Game Microprocessor IC15. These bits are buffered by IC16, IC21, and IC22 to produce the bits on AB0–AB15. They are also used as the address bits for Program ROM IC1–IC4.

AB
Signal AB is the blue playfield data generated at pin 10 of shift register IC140 in the Video Output Decoders circuit when LD/$\overline{SFT}$ goes low. Data into the shift register is multiplexed by IC141 from the playfield dynamic RAM data on DD0–DD3. This occurs when ENA goes high. The AB signal is processed in the Video Output circuit.

AB0–AB15
Address bits on Buffered Microprocessor Address Bus lines AB0–AB15 are software generated by Game Microprocessor IC15 and are buffered by IC16, IC21, and IC22. The bits on lines AB0–AB2 and AB9–AB15 are the select input signals for Address Decoders IC17, IC18, IC31, and IC32. (Refer to the Memory Map to determine which addresses activate the various Address Decoder output signals.)

The bits on lines AB0–AB10 are multiplexed with those on lines OA0–OA10 in the Custom I/O Microprocessor RAM circuit by IC23–IC25 to produce the address bits for IC10.

The bits on lines AB0–AB13 are multiplexed with the output count of IC51, IC70, IC49, and IC68 of the Dynamic RAM Address circuit to produce the bits on ABX0–ABX13 at the outputs of IC52, IC71, IC53, and IC72.

In the Game Microprocessor circuit, AB15 is gated with $\overline{CS1}$ to produce the enable for data-bus buffer IC28.

In the Watchdog Enable circuit, AB14 is one of the control signals used to generate the $\overline{WAIT}$ signal for Game Microprocessor IC15.

$\overline{ABHF}$
The active low-level $\overline{ABHF}$ signal is software-generated by Sound Microprocessor IC27. This signal is gated through IC189 to control the blue shading when the playfield is written.

ABP0–ABP12
The picture ROM address bits on lines ABP0–ABP11 are generated by counters IC46, IC65, and IC47 in the Picture ROM Address Decoders circuit.

The bit on ABP12 is generated by flip-flop IC66. These lines carry the address bits for the Picture ROM.

ABX0–ABX13
The buffered DMA address bits on lines ABX0–ABX13 are generated by multiplexers IC52, IC53, IC71, and IC72 in the Dynamic RAM Address circuit. These bits are the address inputs for Dynamic RAM Multiplexers IC130–IC133.

$\overline{ACAS0}$
The active low-level $\overline{ACAS0}$ signal is generated at pin 8 of IC104 in the Row/Column Address Select circuit. This is the column address select for the Red/Shade Playfield RAM. $\overline{ACAS0}$ is active low when CAS is high.

$\overline{ACAS1}$
The active low-level $\overline{ACAS1}$ signal is generated at pin 6 of IC104 in the Row/Column Address Select circuit. This is the column address select for the Blue/Green Playfield RAM. $\overline{ACAS1}$ is active low when CAS is high.

AG
Signal AG is the green playfield data generated at pin 10 of shift register IC142 in the Video Output Decoders circuit when LD/$\overline{SXT}$ goes low. Data into the shift register is multiplexed by IC143 from the playfield dynamic RAM data on DD4–DD7. This occurs when ENA goes high. The AG signal is processed in the Video Output circuit.

$\overline{AGHF}$
The active low-level $\overline{AGHF}$ signal is software-generated by Sound Microprocessor IC27. This signal is gated through IC99 to control the green shading when the playfield is written.

AR
Signal AR is the red playfield data generated at pin 10 of shift register IC135 in the Video Output Decoders circuit when LD/$\overline{SFT}$ goes low. Data into the shift register is multiplexed by IC134 from the playfield dynamic RAM data on DD0–DD3. This occurs when ENA goes high. The AR signal is processed in the Video Output circuit.

$\overline{ARAS0}$
The active low-level $\overline{ARAS0}$ signal is generated at pin 11 of IC104 in the Row/Column Address Select circuit. This is the row address select for the Red/Shade Playfield RAM. $\overline{ARAS0}$ is active low when RAS is high.

$\overline{ARAS1}$
The active low-level $\overline{ARAS1}$ signal is generated at pin 3 of IC104 in the Row/Column Address Select circuit. This is the row address select for the Blue/Green Playfield RAM. $\overline{ARAS1}$ is active low when RAS is high.

$\overline{ARHF}$
The active low-level $\overline{ARHF}$ signal is software-generated by Sound Microprocessor IC27. This signal is gated through IC99 to control the red shading when the playfield is written.

AV0–AV14
The Video Address bits on lines AV0–AV14 are generated by counters IC95, IC96, and flip-flop IC129 in the Clock, Sync Chain, and Timing Signals circuit. These bits are used to generate $\overline{BLNK}$, $\overline{INT}$, $\overline{VSYNC}$, and $\overline{TRGA}$. In the Dynamic RAM Flip Address circuit, these bits are used to produce the flipped address bits when the game is in the cocktail mode.

$\overline{AV6'}$
The bit on $\overline{AV6'}$ is generated at pin 4 of IC111 in the Clock, Sync Chain, and Timing Signals circuit by inverting the bit on AV6′. This signal functions as a horizontal blanking signal by disabling multiplexers IC141, IC143, IC134, IC136, IC151, IC153, IC144, and IC146 in the Video Output Decoders circuit during video blanking.

AVX0–AVX13
The flipped video address bits on lines AVX0–AVX13 are developed in the Dynamic RAM Flip Addresses circuit from the bits on AV0–AV13. These signals are used, when the game is in the cocktail mode, by Dynamic RAM Multiplexers IC130–IC133.

$\overline{AW0}$–$\overline{AW3}$
The active low-level write enable signals on lines $\overline{AW0}$–$\overline{AW3}$ are generated by IC121 in the Dynamic RAM Write Enable circuit from the bits on DB0–DB4 and DIS0–DIS3. $\overline{AW0}$–$\overline{AW3}$ write enable the Red/Shade Playfield RAM.

AZ
Signal AZ is the playfield shading data generated at pin 10 of shift register IC137 in the Video Output Decoders circuit when LD/$\overline{SFT}$ goes low. Data into the shift register is multiplexed by IC136 from the playfield dynamic RAM data on DD4–DD7. This occurs when ENA goes high. The AZ signal is processed in the Video Output circuit.

BB
Signal BB is the blue motion-object data generated at pin 10 of shift register IC150 in the Video Output Decoders circuit when LD/$\overline{SFT}$ goes low. Data into the shift register is multiplexed by IC151 from the playfield dynamic RAM data on DD0–DD3. This occurs when ENA goes high. The BB signal is processed in the Video Output circuit.

$\overline{BCAS0}$
The active low-level $\overline{BCAS0}$ signal is generated at pin 8 of IC106 in the Row/Column Address Select circuit. This is the column address select for the Red/Shade Motion-Object RAM. $\overline{BCAS0}$ is active low when CAS is high.

$\overline{\text{BCAS1}}$
The active low-level $\overline{\text{BCAS1}}$ signal is generated at pin 6 of IC106 in the Row/Column Address Select circuit. This is the column address select for the Blue/Green Motion-Object RAM. $\overline{\text{BCAS1}}$ is active low when CAS is high.

BG
Signal BG is the green motion-object data generated at pin 10 of shift register IC152 in the Video Output Decoders circuit when LD/$\overline{\text{SFT}}$ goes low. Data into the shift register is multiplexed by IC153 from the playfield dynamic RAM data on DD4–DD7. This occurs when ENA goes high. The BG signal is processed in the Video Output circuit.

$\overline{\text{BLNK}}$
The active low-level Blanking signal is generated at pin 6 of IC108 in the Clock, Sync Chain, and Timing Signals circuit. $\overline{\text{BLNK}}$ is used in the Video Output circuit to turn off gates IC118, IC119, IC120, IC189, IC98, and IC99 during video blanking.

BR
Signal BR is the red motion-object data generated at pin 10 of shift register IC145 in the Video Output Decoders circuit when LD/$\overline{\text{SFT}}$ goes low. Data into the shift register is multiplexed by IC144 from the playfield dynamic RAM data on DD0–DD3. This occurs when ENA goes high. The BR signal is processed in the Video Output circuit.

$\overline{\text{BRAS0}}$
The active low-level $\overline{\text{BRAS0}}$ signal is generated at pin 11 of IC106 in the Row/Column Address Select circuit. This is the row address select for the Red/Shade Motion-Object RAM. $\overline{\text{BRAS0}}$ is active low when RAS is high.

$\overline{\text{BRAS1}}$
The active low-level $\overline{\text{BRAS1}}$ signal is generated at pin 3 of IC106 in the Row/Column Address Select circut. This is the row address select for the Blue/Green Motion-Object RAM. $\overline{\text{BRAS1}}$ is active low when RAS is high.

$\overline{\text{BSEL}}$
$\overline{\text{BSEL}}$ is software-generated by Address Decoder IC31. $\overline{\text{BSEL}}$ is the clock signal for flip-flops IC90 of the Row/Column Address Select circuit.

$\overline{\text{BW0}}$–$\overline{\text{BW3}}$
The active low-level write enable signals on $\overline{\text{BW0}}$–$\overline{\text{BW3}}$ are generated by IC122 in the Dynamic RAM Write Enable circuit. These signals write enable the Blue/Green Playfield RAM.

BZ
Signal BZ is the motion-object shading data generated at pin 10 of shift register IC147 in the Video Output Decoders circuit when LD/$\overline{\text{SFT}}$ goes low. Data into the shift register is multiplexed by IC146 from the playfield dynamic RAM data on DD3–DD7. This occurs when ENA goes high. The BZ signal is processed in the Video Output circuit.

CAS
The active high-level Column Address Select enable signal is generated at pin 8 of IC125 in the Clock, Sync Chain, and Timing Signals circuit. CAS enables IC104 and IC106 for dynamic RAM column select in the Row/Column Address Select circuit.

$\overline{\text{CLK4}}$
The $\overline{\text{CLK4}}$ signal is generated at pin 9 of IC91 in the Clock, Sync Chain, and Timing Signals circuit. This is the clock signal for Custom I/O Microprocessor IC26, via buffer IC38.

$\overline{\text{COM0}}$–$\overline{\text{COM5}}$
The active low-level $\overline{\text{COM0}}$–$\overline{\text{COM5}}$ signals are software-generated by Custom I/O Microprocessor IC26. These signals are the output enables for buffers IC11–IC13 in the Input Bus Drivers circuit.

$\overline{\text{CW0}}$–$\overline{\text{CW3}}$
The active low-level write enable signals on $\overline{\text{CW0}}$–$\overline{\text{CW3}}$ are generated by IC123 in the Dynamic RAM Write Enable circuit. These signals write enable the Red/Shade Motion-Object RAM.

D0–D7
Microprocessor Data Bus lines D0–D7 form a bi-directional data bus between the Game Microprocessor, the Program ROM, the microprocessor data-bus buffer (IC28), and the Custom I/O Microprocessor RAM buffer (IC9).

DB0–DB7
Buffered Microprocessor Data Bus lines DB0–DB7 form a bi-directional data bus between microprocessor data-bus buffer (IC28), the Coin and DIP Switch Inputs, the Sound Microprocessor, the Dynamic RAM Address, the Picture ROM Address Decoders, the Row/Column Address Select, the DMA Control, and the Dynamic RAM Data circuits.

DD0–DD7
Lines DD0–DD7 form a data bus from the dynamic RAM in the Red/Shade Playfield RAM, Blue/Green Playfield RAM, Red/Shade Motion-Object RAM, and Blue/Green Motion-Object RAM circuits to decoders IC134, IC136, IC141, IC143, IC144, IC146, IC151, and IC153 in the Video Output Decoders circuit.

$\overline{\text{DIS0}}$–$\overline{\text{DIS3}}$
The active low-level enable signals on $\overline{\text{DIS0}}$–$\overline{\text{DIS3}}$ are generated by IC103 in the Enable Control Logic circuit. These signals are produced from the picture ROM data and are used to control the outputs of IC121–IC124 in the Dynamic RAM Write Enable circuit.

DPB0–DPB3
The blue data bits on lines DPB0–DPB3 are generated by Picture ROM ICGB0 and ICGB1. These bits are multiplexed with DB0–DB3 by IC45 in the Dynamic RAM Data circuit. When EXCT is high, the bits on DPB0–DPB3 are used to generate those on DXB0–DXB3. In the Enable Logic Control circuit, the bits on DPB0–DPB3 are gated by IC100.

DPG0–DPG3
The green data bits on lines DPG0–DPG3 are generated by Picture ROM ICGB0 and ICGB1. These bits are multiplexed with DB4–DB7 by IC64 in the Dynamic RAM Data circuit. When EXCT is high, the bits on DPG0–DPG3 are used to generate those on DXG0–DXG3. In the Enable Logic Control circuit, the bits on DPG0–DPG3 are gated by IC100.

DPR0–DPR3
The red data bits on lines DPR0–DPR3 are generated by Picture ROM ICZR0 and ICZR1. These bits are multiplexed with DB0–DB3 by IC48 in the Dynamic RAM Data circuit. When EXCT is high, the bits on DPR0–DPR3 are used to generate those on DXR0–DXR3. In the Enable Logic Control circuit, the bits on DPR0–DPR3 are gated by IC102.

DPZ0–DPZ3
The shading data bits on lines DPZ0–DPZ3 are generated by Picture ROM ICZR0 and ICZR1. These bits are multiplexed with DB4–DB7 by IC67 in the Dynamic RAM Data circuit. When EXCT is high, the bits on DPZ0–DPZ3 are used to generate those on DXZ0–DXZ3. In the Enable Logic Control circuit, the bits on DPG0–DPG3 are gated by IC101.

$\overline{\text{DW0}}$–$\overline{\text{DW3}}$
The active low-level write enable signals on $\overline{\text{DW0}}$–$\overline{\text{DW3}}$ are generated by IC124 in the Dynamic RAM Write Enable circuit. These signals write enable the Blue/Green Motion-Object RAM.

DXB0–DXB3
The multiplexed blue data bits on DXB0–DXB3 are generated by IC45 in the Dynamic RAM Data circuit. These are input to blue playfield RAM IC174–IC177 and to blue motion-object RAM IC182–IC185.

DXG0–DXG3
The multiplexed green data bits on DXG0–DXG3 are generated by IC64 in the Dynamic RAM Data circuit. These are input to green playfield RAM IC158–IC161 and to green motion-object RAM IC166–IC169.

DXR0–DXR3
The multiplexed red data bits on DXR0–DXR3 are generated by IC48 in the Dynamic RAM Data circuit. These are input to red playfield RAM IC170–IC173 and to red motion-object RAM IC178–IC181.

DXZ0–DXZ3
The multiplexed shading data bits on DXZ0–DXZ3 are generated by IC67 in the Dynamic RAM Data circuit. These are input to shading playfield RAM IC154–IC157 and to shading motion-object RAM IC162–IC165.

ENA
The active high-level ENA signal is software-generated by Sound Microprocessor IC27. This signal enables the playfield color multiplexers of the Video Output Decoders circuit via gate IC191.

ENB
The active high-level ENB signal is software-generated by Sound Microprocessor IC27. This signal enables the motion-object color multiplexers of the Video Output Decoders circuit via gate IC191.

EXCT
The active high-level EXCT signal is developed from the DMA start signal (at pin 8 of IC55 in the DMA Control circuit) by IC54 and IC58. EXCT enables trickle input to counter IC43 in the DMA Control circuit, and to counters IC49 and IC51 in the Dynamic RAM Address circuit. In the Dynamic RAM Address circuit, EXCT also selects the address bus for input to multiplexers IC53, IC72, IC52, and IC71.

In the Watchdog Enable circuit, EXCT is used to help generate $\overline{\text{WAIT}}$. In the Dynamic RAM Data circuit, EXCT selects the picture data bits for output from IC45, IC48, IC64, and IC67.

$\overline{\text{EXCT}}$
The active low-level $\overline{\text{EXCT}}$ signal is developed from the DMA start signal (at pin 8 of IC55 in the DMA Control circuit) by IC73. $\overline{\text{EXCT}}$ is the chip select for the Picture ROM. In the Row/Column Address Select circuit, $\overline{\text{EXCT}}$ controls the output of gates IC110 for dynamic RAM row and column selects. In the Picture ROM Address Decoders circuit, this signal enables the trickle input to counter IC46.

GATE ENABLE
The GATE ENABLE signal is clocked out of the Watchdog Enable circuit by $\overline{\text{K2}}$ at IC91. This signal enables the logic gates at IC108 for the dynamic RAM row and column select logic.

IN0–IN3
The data bits on IN0–IN3 are hardware-generated by the control panel and buffered by IC11–IC13 in the Input Bus Drivers circuit. These data bits are input to Custom I/O Microprocessor IC26.

$\overline{\text{IN0}}$, $\overline{\text{IN1}}$
The active low-level Input Address Select lines are software-generated by Address Decoder IC32. These are the select enables for IC41 and IC61 in the Coin & DIP Switch Inputs circuit. When low, $\overline{\text{IN0}}$ enables the COIN R INPUT and COIN L INPUT data through IC41 to DB0 and DB1, and the SELF TEST and Service Switch data through IC61 to DB2 and DB3. When low, $\overline{\text{IN1}}$ enables the data from DIP switch SW1 to pass through IC41 and IC61 to the data bus.

$\overline{\text{INT}}$
The active low-level Interrupt Request is generated every 16 ms at pin 3 of IC92 in the Clock, Sync Chain, and Timing Signals circuit. After inversion by IC75 of the Game Microprocessor cicuit, it clocks through D-type flip-flop IC74 into pin 16 of Game Microprocessor IC15.

$\overline{\text{IREQ}}$
The active low-level Interrupt Request signal is software-generated by Sound Microprocessor IC27. This signal is the Interrupt Request for Custom I/O Microprocessor IC26.

K1
The active high-level K1 signal is generated at pin 7 of IC80 in the Clock, Sync Chain, and Timing Signals circuit. KI is used by IC80 to produce the dynamic RAM column address enable signal (CAS).

$\overline{\text{K1}}$
The active low-level $\overline{\text{K1}}$ signal is generated at pin 4 of IC77 in the Clock, Sync Chain, and Timing Signals circuit. This is a DMA timing signal for clocking IC49, IC68, IC51, and IC70 in the Dynamic RAM Address circuit; IC46, IC65, and IC47 in the Picture ROM Address Decoders circuit; and IC34, IC43, and IC62 in the DMA Control circuit. $\overline{\text{K1}}$ is gated by IC57 and IC58 in the Custom I/O Microprocessor Read/Write circuit to produce the clock for flip-flops IC39.

$\overline{\text{K1S1}}$
The active low-level $\overline{\text{K1S1}}$ signal is generated at pin 8 of IC78 in the Clock, Sync Chain, and Timing Signals circuit from K1. In the DMA Control circuit, $\overline{\text{K1S1}}$ is gated with K2 to clock IC55.

K2
The active high-level K2 signal is generated at pin 2 of IC77 in the Clock, Sync Chain, and Timing Signals circuit. K2 enables parallel counts at IC46, IC65, and IC47 in the Picture ROM Address Decoders circuit; IC62 IC43, IC54, and IC74 in the DMA Control circuit; and IC70, and IC51 in the Dynamic RAM Address circuit.

$\overline{\text{K2}}$
The active low-level $\overline{\text{K2}}$ signal is generated at pin 6 of IC77 in the Clock, Sync Chain, and Timing Signals circuit. $\overline{\text{K2}}$ controls Dynamic RAM Multiplexers IC130–IC133 via gate IC111. It also is the clock signal for Sound Microprocessor IC27.

$\overline{\text{LDL}}$
The active low-level $\overline{\text{LDL}}$ signal is generated at pin 11 of IC73 in the DMA Control circuit. $\overline{\text{LDL}}$ parallel loads counters IC43 and IC62 in the DMA Control circuit and counters IC51 and IC70 in the Dynamic RAM Address circuit. $\overline{\text{LDL}}$ is inverted by IC75 in the Dynamic RAM Address circuit to enable a parallel count from IC68 and IC49.

LD/$\overline{\text{SFT}}$
The LD/$\overline{\text{SFT}}$ signal is generated at pin 8 of IC58 in the Clock, Sync Chain, and Timing Signals circuit. When high, LD/$\overline{\text{SFT}}$ loads the dynamic RAM data from the multiplexers of the Video Output Decoders circuit to the associated shift register. When low, it shifts this data out of the shift registers to the Video Output circuit.

$\overline{\text{MR}}$
The active low-level Microprocessor Read signal is generated at pin 11 of IC20 when the Game Microprocessor is reading from the data bus. $\overline{\text{MR}}$ occurs when both $\overline{\text{MREQ}}$ and pin 21 of IC15 are low.

In the Address Decoders circuit, $\overline{\text{MR}}$ enables IC32. In the Watchdog circuit, $\overline{\text{MR}}$ is decoded with other control signals to produce $\overline{\text{WAIT}}$. In the Game Microprocessor circuit, it is gated with $\overline{\text{PRD}}$ by IC54 to produce the direction signal for data-bus buffer IC28. In the Program ROM circuit, $\overline{\text{MR}}$ is the output enable signal for IC1–IC4. In the Custom I/O Microprocessor RAM circuit, $\overline{\text{MR}}$ is gated through IC56 and IC35 to enable IC10.

$\overline{\text{MREQ}}$
The active low-level Memory Request signal is generated by Game Microprocessor IC15 and buffered by IC19. This signal indicates that the bits on the microprocessor address bus are valid for a read or write operation. $\overline{\text{MREQ}}$ is gated with the active $\overline{\text{RD}}$ or $\overline{\text{WR}}$ output from the Game Microprocessor to enable IC20 to produce $\overline{\text{MR}}$ or $\overline{\text{MW}}$. $\overline{\text{MREQ}}$ is also used to enable IC75 and IC187 of the Watchdog Enable circuit.

$\overline{\text{MW}}$
The active low-level Microprocessor Write signal is generated at pin 3 of IC20 when the Game Microprocessor is writing to the data bus. $\overline{\text{MW}}$ occurs when both $\overline{\text{MREQ}}$ and pin 22 of IC15 are low.

In the Address Decoders circuit, $\overline{\text{MW}}$ is the enable signal for IC31. In the Watchdog Enable circuit, $\overline{\text{MW}}$ is decoded with other control signals to produce $\overline{\text{WAIT}}$. In the Custom I/O Microprocessor RAM circuit, $\overline{\text{MW}}$ is used to enable IC10 for a write operation (via gates IC56 and IC35) and also determines the direction of data flow through buffer IC9.

OA0–OA10
The address bits on OA0–OA10 are generated by Custom I/O Microprocessor IC26. These bits are multiplexed by IC23–IC25 to produce the address for Custom I/O Microprocessor RAM IC10.

$\overline{\text{OR}}$
The active low-level $\overline{\text{OR}}$ signal is generated at pin 8 of IC56 in the Custom I/O Microprocessor Read/Write circuit whenever Custom I/O Microprocessor IC26 requests a read from IC10. $\overline{\text{OR}}$ is gated by IC35 to enable the Custom I/O Microprocessor RAM (IC10). It also clocks flip-flops IC37 to pass data into the Custom I/O Microprocessor.

$\overline{\text{OW}}$
The active $\overline{\text{OW}}$ signal is generated at pin 3 of IC56 in the Custom I/O Microprocessor Read/Write circuit whenever Custom I/O Microprocessor IC26 requests to write data to IC10. $\overline{\text{OW}}$ is gated by IC35 to write enable IC10. $\overline{\text{OW}}$ enables Custom I/O Microprocessor buffer IC36 via inverter IC57.

PRD
The active low-level Priority Read signal is generated at pin 11 of IC187 whenever the Game Microprocessor requests to read data from the data bus. $\overline{\text{PRD}}$ is gated with $\overline{\text{MR}}$ by IC54 to determine the direction of data flow through data-bus buffer IC28. $\overline{\text{PRD}}$ also is a control signal for the output logic gates of Sound Microprocessor IC27.

$\overline{\text{PROM ENABLE}}$
The $\overline{\text{PROM ENABLE}}$ signal is generated by flip-flop IC66 in the Picture ROM Address Decoders circuit from the data on DB4. When low, $\overline{\text{PROM ENABLE}}$ enables an output from Picture IC84 and IC85. When high, it is inverted to enable an output from Picture ROM IC86 and IC87.

$\overline{\text{PWR}}$
The active low-level Priority Write signal is generated at pin 3 of IC187 whenever the Game Microprocessor requests to write data to the data bus. $\overline{\text{PWR}}$ is a control signal that enables Sound Microprocessor IC27 for output.

RAS
The active high-level Row Address Select enable signal is generated at pin 6 of IC76 in the Clock, Sync Chain, and Timing Signals circuit. RAS is gated by IC77 and IC58 to develop LD/$\overline{\text{SXT}}$. In the Row/Column Address Select circuit, RAS enables IC104 and IC106 for dynamic RAM row select.

RB0–RB3
The data bits on RB0–RB3 are generated by Custom I/O Microprocessor IC26 and buffered by IC36. These data bits are latched by IC37 to provide the input data bits for the Custom I/O Microprocessor. In addition, RB0–RB3 are sent to Custom I/O Microprocessor RAM IC10.

RD
The RD signal is generated by Custom I/O Microprocessor IC26. RD enables buffer IC38 in the Custom I/O Microprocessor circuit and logic gates IC35 in the Custom I/O Microprocessor Read/Write circuit. RD is the data input for IC40, which uses it to produce $\overline{\text{OR}}$.

$\overline{\text{RD(H)}}$
The active low-level $\overline{\text{RD(H)}}$ signal is software-generated by Address Decoder IC31. $\overline{\text{RD(H)}}$ clocks flip-flop IC66 and parallel loads counter IC47 for the high address byte of picture ROM data for DMA in the Picture ROM Address Decoders circuit.

$\overline{\text{RD(L)}}$
The active low-level $\overline{\text{RD(L)}}$ signal is software-generated by Address Decoder IC31. $\overline{\text{RD(L)}}$ parallel loads buffered data into IC46 and IC65 in the Picture ROM Address Decoders circuit for the picture ROM data low-byte address for DMA.

$\overline{\text{RESET}}$
The active low-level $\overline{\text{RESET}}$ signal is generated by transistor TR3 in the Game Microprocessor circuit. This is the reset signal for Game Microprocessor IC15, Sound Microprocessor IC27, and Custom I/O Microprocessor IC26. In the Custom I/O Microprocessor RAM Control circuit, it presets flip-flop IC59.

$\overline{\text{ROM0}}$–$\overline{\text{ROM3}}$
The active low-level Read-Only Memory Chip Select lines $\overline{\text{ROM0}}$–$\overline{\text{ROM3}}$ are software-generated by address Decoder IC17. These are the chip select signals for Program ROM IC1–IC4.

SELI/$\overline{\text{II}}$
The SELI/$\overline{\text{II}}$ signal is software-generated by Custom I/O Microprocessor IC26. This signal is used in the Dynamic RAM Flip Addresses circuit to flip the video for a cocktail game. In the Video Output Decoders circuit, SELI/$\overline{\text{II}}$ is inverted by IC75 to produce the data select signal for multiplexers IC134, IC136, IC141, IC143, IC146, IC151, and IC153.

$\overline{\text{SFT}}$
The active low-level $\overline{\text{SFT}}$ signal is generated by IC80 and inverted by IC60 in the Clock, Sync Chain, and Timing Signals circuit. $\overline{\text{SFT}}$ enables shift registers IC135, IC137, IC140, IC142, IC145, IC147, IC150, and IC152 of the Video Output Decoders circuit to be loaded or shifted, depending on the state of LD/$\overline{\text{SFT}}$.

$\overline{\text{SG0}}$, $\overline{\text{SG1}}$
The active low-level Sound Generation signals are software-generated by Address Decoder IC32. $\overline{\text{SG0}}$ control the address and data latch select logic gates for Sound Microprocessor IC27. $\overline{\text{SG1}}$ controls the input/output select logic gates for Sound Microprocessor IC27.

$\overline{\text{SRES}}$
The active low-level Sound Reset signal is software-generated by Sound Microprocessor IC27. $\overline{\text{SRES}}$ is gated with $\overline{\text{RESET}}$ by IC58 to control the reset input of Custom I/O Microprocessor IC26.

$\overline{\text{TRGA}}$
The active low-level horizontal sync signal ($\overline{\text{TRGA}}$) is generated at pin 8 of IC129 in the Clock, Sync Chain, and Timing Signals circuit. $\overline{\text{TRGA}}$ clears IC96 and is gated through IC120 for further processing by the video display.

$\overline{\text{VSYNC}}$
The active low-level Vertical Sync signal is generated at pin 8 of IC94 in the Clock, Sync Chain, and Timing Signals circuit. $\overline{\text{VSYNC}}$ is gated by IC120 in the Video Output circuit to develop COMPSYNC. $\overline{\text{VSYNC}}$ is inverted by IC188 to produce VSYNC for further processing by the video display.

$\overline{\text{WAIT}}$
The active low-level Wait signal is generated at pin 8 of IC128 by decoding the control signals input to the Watchdog Enable circuit. $\overline{\text{WAIT}}$ is buffered by IC19 and applied to pin 24 of the Game Microprocessor, IC15.

WE
The active high-level Write Enable signal is generated at pin 9 of IC133 in the Dynamic RAM Multiplexer circuit. This is the signal that enables IC105 in the Dynamic RAM Write Enable circuit.

WR
The WR signal is generated by Custom I/O Microprocessor IC26. WR enables logic gates IC35 to produce the chip select for Custom I/O Microprocessor RAM IC10. In the Custom I/O Microprocessor Read/Write circuit, WR is the data input for IC40, which uses it to produce $\overline{\text{OW}}$.

$\overline{WR}(\overline{H})$
The active low-level $\overline{WR}(\overline{H})$ signal is software-generated by Address Decoder IC31. $\overline{WR}(\overline{H})$ parallel loads buffered data into IC49 and IC68 in the Dynamic RAM Address circuit for the bit map RAM high-byte starting address for DMA.

$\overline{WR}(\overline{L})$
The active low-level $\overline{WR}(\overline{L})$ signal is software-generated by Address Decoder IC31. $\overline{WR}(\overline{L})$ clocks IC69 and IC50 to pass data to counters IC70 and IC51 in the Dynamic RAM Address circuit for the bit map RAM low-byte starting address for DMA.

XA0–XA6
The dynamic RAM address bits on lines XA0–XA6 are generated by the Dynamic RAM Multiplexers and used to address the Red/Shade Playfield RAM, the Blue/Green Playfield RAM, the Red/Shade Motion-Object RAM, and the Blue/Green Motion-Object RAM.

XGH/$\overline{L}$
The XGH/$\overline{L}$ signal is generated at pin 8 of IC76 in the Clock, Sync Chain, and Timing Signals circuit. This signal is used by the Dynamic RAM Multiplexers (IC130–IC133) to flip the video by selecting flip video addresses.

$\overline{XY}(\overline{H})$
The active low-level $\overline{XY}(\overline{H})$ signal is software-generated by Address Decoder IC31. $\overline{XY}(\overline{H})$ presets flip-flop IC55 in the DMA Control circuit for the picture size high-byte and DMA start.

$\overline{XY}(\overline{L})$
The active low-level $\overline{XY}(\overline{L})$ signal is software-generated by Address Decoder IC31. $\overline{XY}(\overline{L})$ clocks flip-flops IC44 and IC63 in the DMA Control circuit for the picture size low-bytes and DMA starts.

Φ
The Φ signal is generated by IC80 in the Clock, Sync Chain, and Timing Signals circuit at a 2.5 MHz rate. This signal is inverted by IC77. Φ clocks Game Microprocessor IC15 through buffer IC36. It is also used to clock data into Custom I/O Microprocessor RAM IC10 via flip-flop IC59.