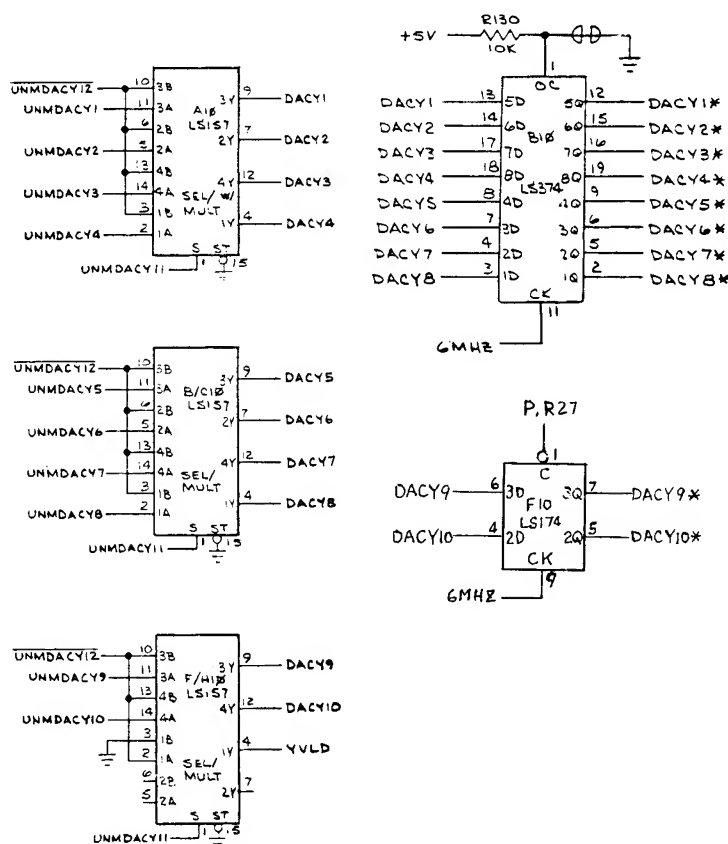
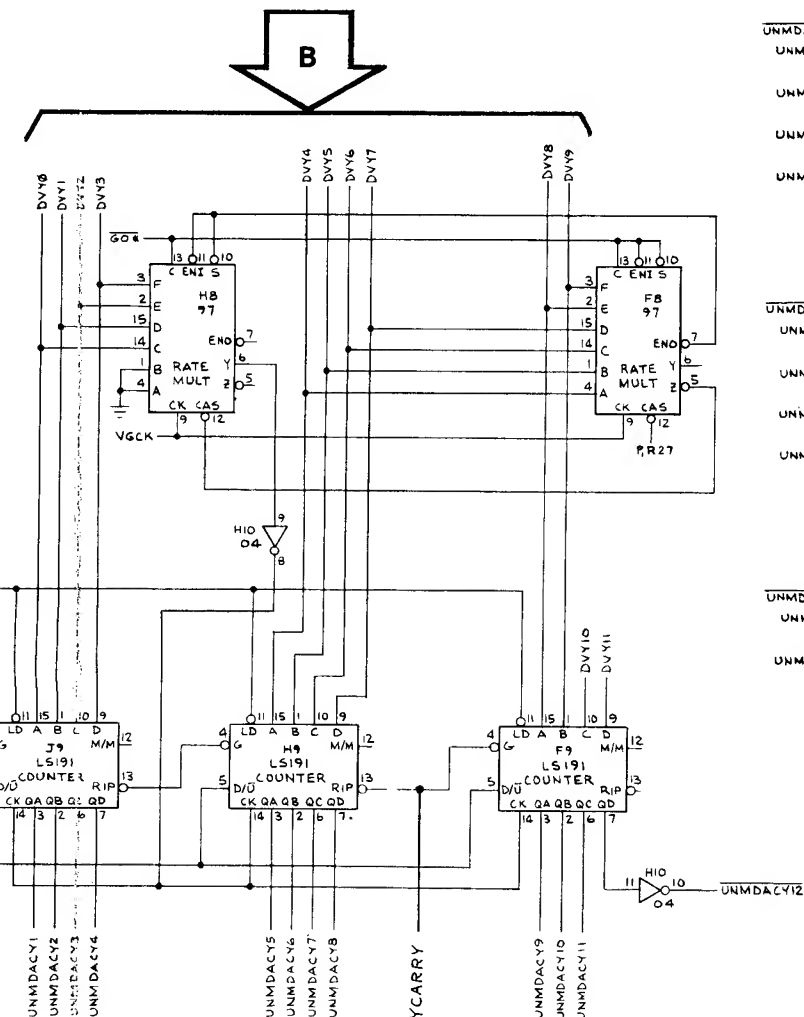




ers count up or down. DVX11 is used
multiplexers D10, E10, and F10.

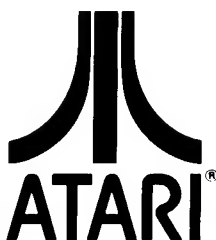
AX10 (X axis unmultiplexed digital) are transferred to the output of the outputs of the latches on each rising of the microcomputer clock circuitry). Signals are sent to the digital-to-analog eq output.

outputs represent the physical placement. The far left of the monitor screen is 0 and the far right is 1023. Therefore, if the position was greater than 1023, the monitor would start at the right side of the screen and start again on the left side under a "wraparound" condition. To prevent a wraparound, a select input from UNMDACX11 goes to the multiplexers to the DACs, forcing the DACs to output values less than 1023 or less than 0. This selects the DACs to output 0, thus keeping the beam on the left side of the screen instead of allowing it to wraparound. The DACs output (valid) outputs from the X and Y positioners are latched and gated together to enable the monitor to display (valid).

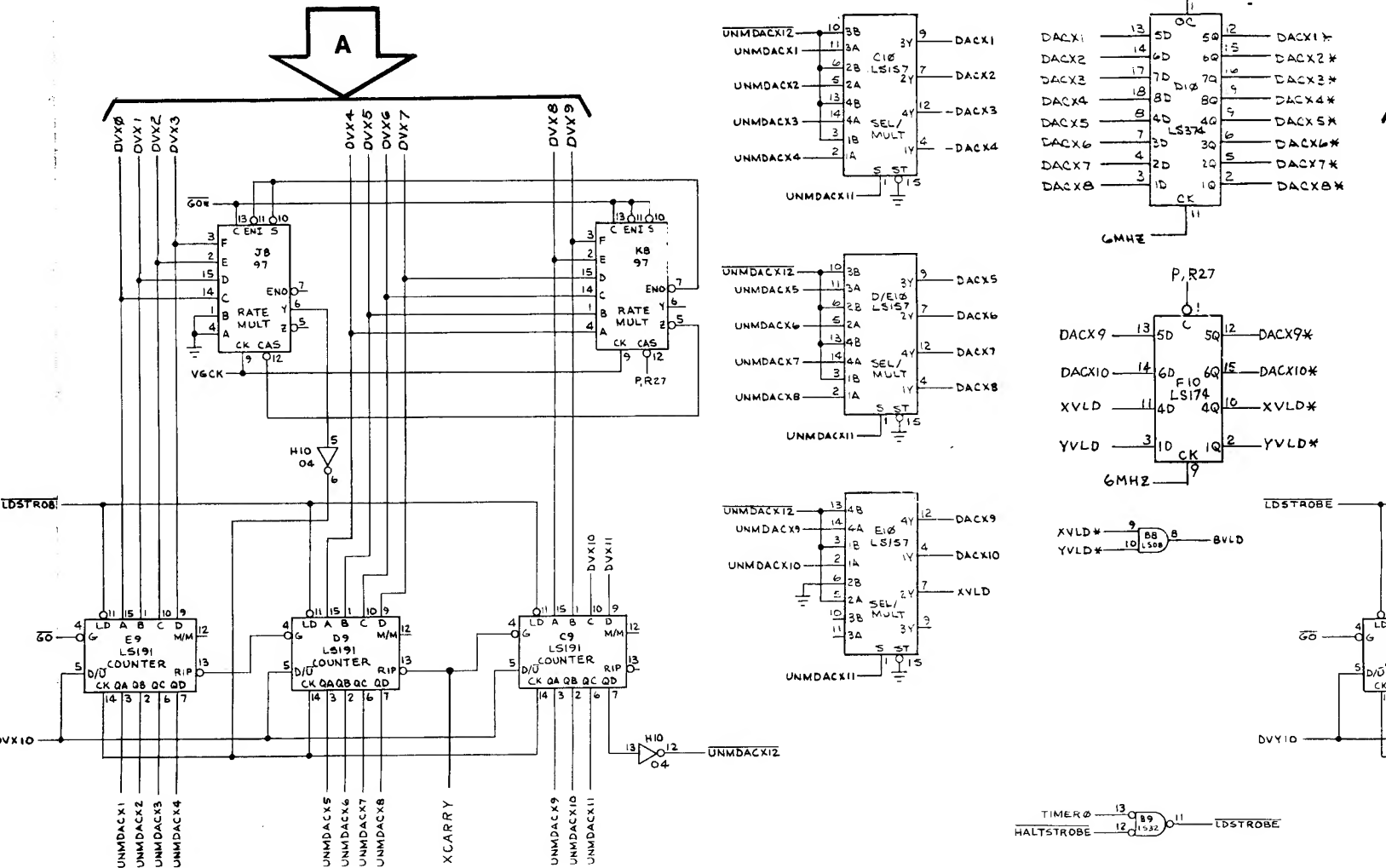
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Sheet 2, Side A

COCKTAIL ASTEROIDS
Video Generator
Section of 034986-XX G



X AND Y POSITION COUNTERS



"jumping" to this new position, the beam itself is turned off to prevent unwanted lines from appearing on the screen. To preset this new position into the counters, the state generator causes LDSTROBE to go low. At this time, a new 12-bit number (DVX0-11) is loaded into the counters from the vector generator memory data latches.

The state machine can also instruct these counters to count up or down any specific number of counts. This will cause the beam to move to the left or to the right a specific distance relative to where it was. During this beam movement, the beam is turned on with the desired intensity. This is the procedure used to draw a vector on the monitor screen. The direction (to the left or right) and length (0 to 1023) of the vector to be drawn relative to the beam's current position is determined by DVX0-11 (from the vector generator memory data latches). This data contains information that determines how many clock pulses the counters will receive and whether the counters will count up or down.

DVX0-9 memory data is loaded into rate multipliers J8 and K8. The function of these devices is to space the desired number of counter clock pulses at equal intervals over the time period that it will take to draw the desired vector. This insures that vectors of different lengths will still be displayed with the same relative beam intensity. DVX10 and 11 are loaded directly into the counters. DVX10

determines whether the counter to control the select input of m

The UNMDACX1 thru UNMDA to-analog converter signals) are multiplexers and stored at the o edge of the 6 MHz clock (from t

The DACX1* thru DACX10* sign converters (DACs) in the X vide ment of the beam on the monito is 0, the center is 512, and the DACX1* thru DACX10* signal v beam would go off the right sid the left side of the screen, a "w wraparound, the multiplexers' s high when the count is greater t UNMDACX12 to be output from ing all zeros or all ones, and t appropriate side on the screen, in

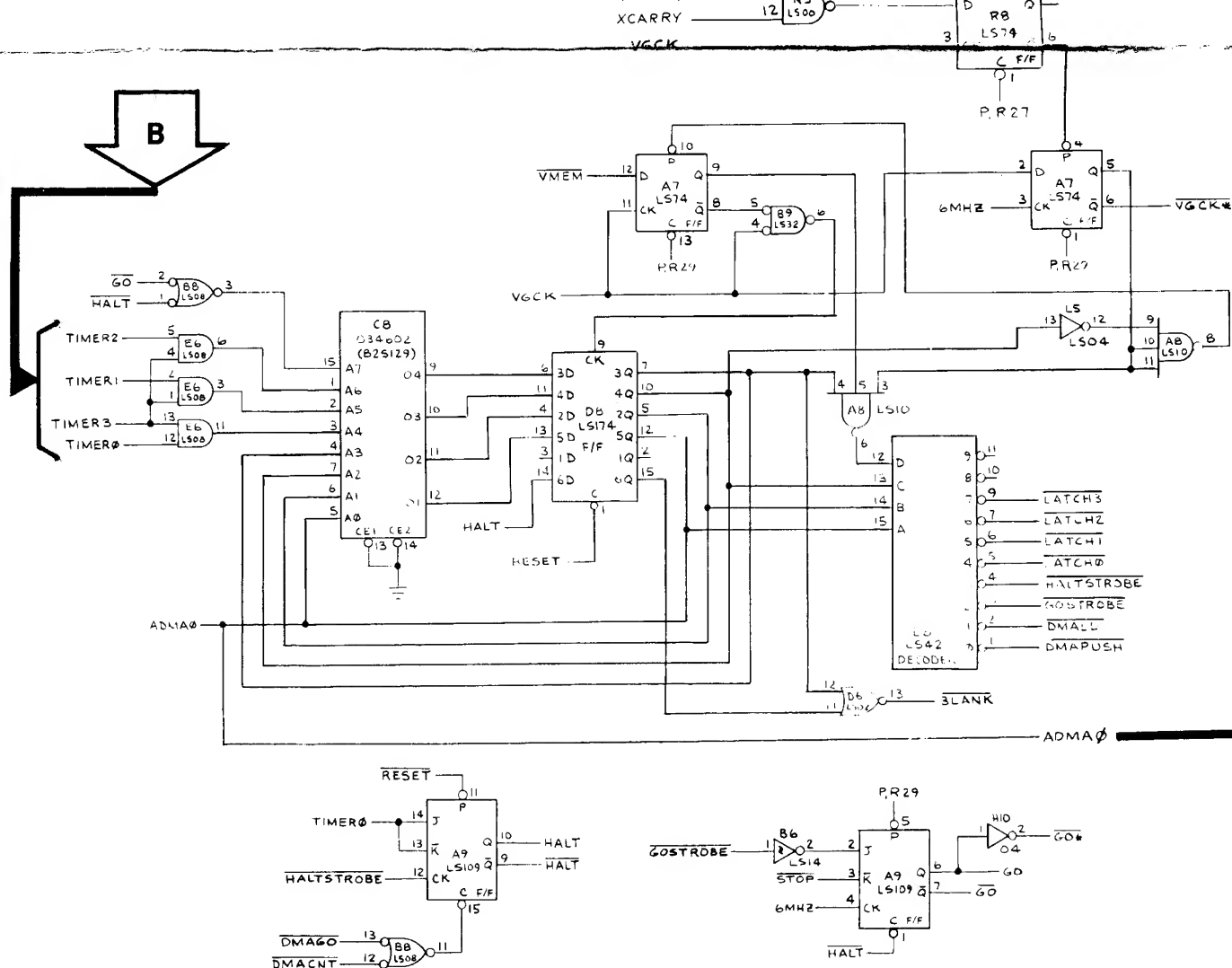
The XVLD and YVLD (X and Y tion counter multiplexers are la the Z axis output, BVLD (beam



60 --

DVX10 —

The state machine can preset this different number from their previous scan beam to "jump" to a new location or, instantaneously, i.e., for drawing a new vector position than where the previous vector



STATE MACHINE

The state machine is the "master controller" of the vector generator circuitry. It receives instructions from the game MPU, via the vector generator RAM. It carries out these instructions by accessing the appropriate sections of the vector generator ROM memory, using the vector generator program counter to do so. The state machine reads the vector generator ROM data (via Timer 0-3) and decodes this information to determine how it should use this data: 1) to draw a vector; 2) to move the monitor beam to a new position on the monitor display; 3) to "jump" to a new vector memory address; 4) to return to a previous vector memory address; or 5) to tell the game MPU that it has completed its current instructions, and is waiting for its next command.

The state machine consists of input gates B8 and E6, ROM C8, latch D8, clock circuitry A7, and decoder E8. Four bit input TIMER0 thru TIMER3 is the operation code input to the state machine. The A4 thru A6 address input to ROM C8 tells the ROM which instructions to perform. Address inputs A0 thru A3 from latch D8 tells the ROM which state was last performed. The address A7 input GO tells the ROM that the position counters are presently drawing a vector. The HALT input to A7 tells the ROM that the vector generator has completed its operations.

During initial power-up of the game, the HALT signal is preset low. The microcomputer reads the high HALT signal through its switch input port (buffer M10) on data line DB0. This tells the microcomputer that the vector generator is halted and waiting for an instruction. To ensure that the beam is off when the state machine is halted, the high HALT, clock-

ed through latch D8, results in a low BLANK to the Z axis output.

The microcomputer outputs an address that results in a DMAGO signal that causes HALT to go high, and clears the vector generator data latches. This makes TIMER0 thru TIMER3 signals all low. The state machine now begins executing instructions, starting at vector memory location 0.

When the state machine receives the operation code for a HALT instruction, it outputs a low HALTSTROBE, setting the HALT flip-flop A9, and suspending state machine operation.

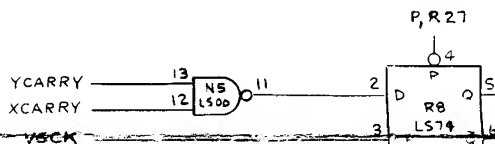
The GO signals load and enable the vector timer and the X and Y position counters and tell the ROM that the vector generator is now actively drawing a vector. The HALT input to GO flip-flop A9 sets the outputs to ensure that the vector timer and position counters are not active when the state machine is halted. When a low GOSTROBE is clocked through A9, the vector timer and X and Y position counters begin to operate from the GO, GO and GO* signals. When STOP is clocked through A9, the vector timer has reached its maximum count, and GO goes high. This means the vector has been drawn.

The VGCK input to the clock circuitry is a buffered 1.5 MHz clock signal from the microcomputer. This is the same frequency used to clock the MPU of the microcomputer. The signal clocks latch D8 unless the microcomputer is addressing the vector RAM or ROM memories (when VMEM goes low). Then the clock input to latch D8 goes high and stays high until VMEM goes high.

[illegible]

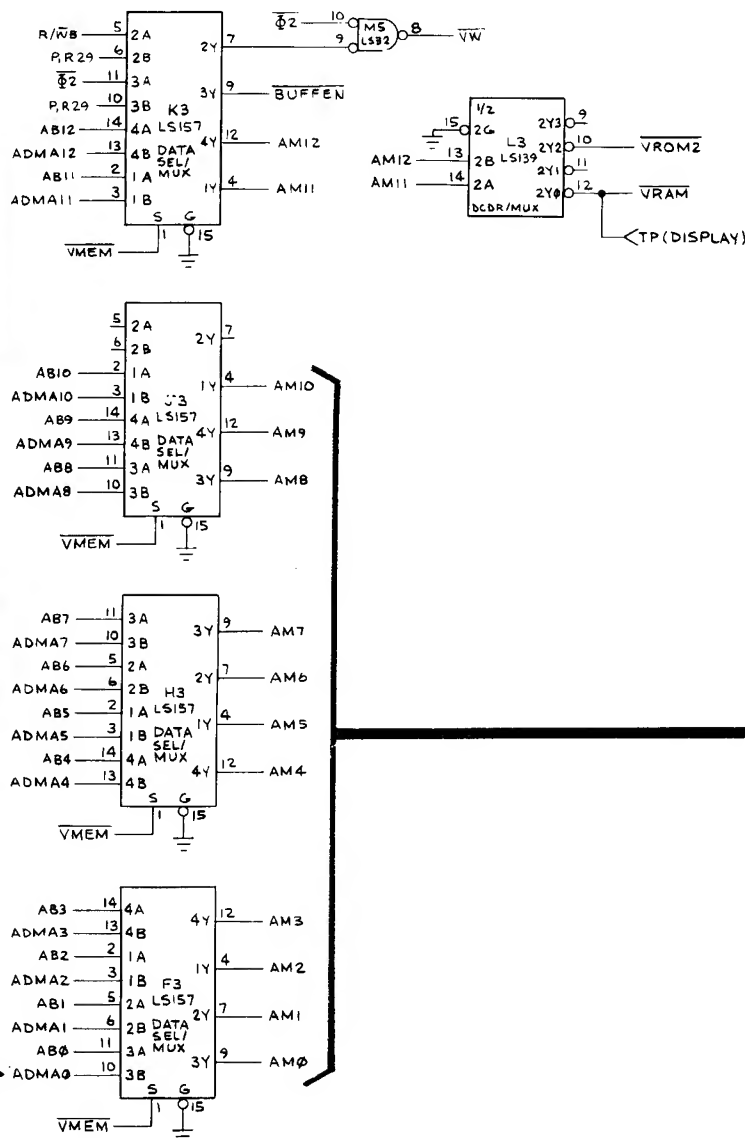
The program counter may also be preset to “jump” to a new address. This new address can be loaded into the program counter from the vector generator memory via

The program counter may also be preset to “return” to a previous address which it had stored in its “stack”. The stack consists of register files F4, H4, & J4, and down/up counter K5. The stack is a 4-word 12-bit memory, used to save the contents of the program counter for future reference. It is loaded when DMAPUSH is low. Immediately after information is written into the stack, counter K5 increments one count. Immediately before loading the program counter from the stack, counter K5 decrements one count.



FROM
MICROCOMPUTER
SHEET 1, SIDE B

VECTOR GENERATOR MEMORY ADDRESS SELECTOR



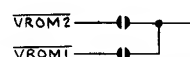
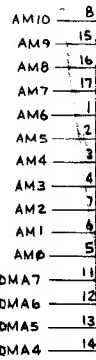
The address selector consists of multiplexers F3, H3, J3 and K3. When $\overline{VMEM}$ is low, the MPU of the microcomputer gains access to the address inputs of the vector generator memory. In this state, $\overline{BUFFEN}$ is from $\overline{\Phi 2}$ and $\overline{VW}$ (vector generator write) is low when $\overline{\Phi 2}$ and $\overline{R/WB}$ are both low. When $\overline{VMEM}$ is high, the address input to the vector generator memory is from the vector generator program counter and state machine. In this state, $\overline{BUFFEN}$ and $\overline{VW}$ are both held high by the pullup resistors connected to the 2B and 3B inputs of multiplexer K3.

Address decoder L3 decodes address bits A11 and A12, and selects the RAM or one of three ROMs of the vector generator memory.

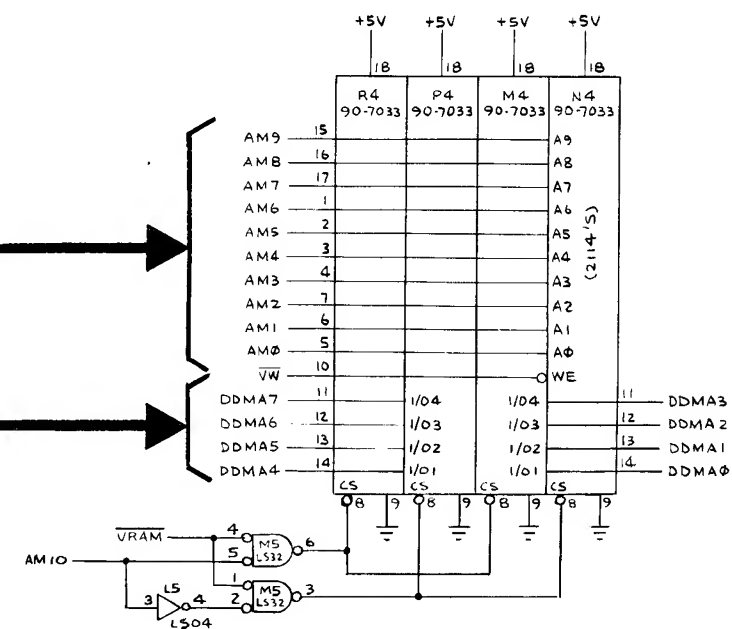
This address-selecting arrangement allows the game MPU to access the vector generator memory, i.e., write data into the vector generator RAM to instruct the vector generator what it should do next. The address selector can then allow the vector generator program counter and state machine to access this same area of RAM also, and read what instructions were sent to it by the game MPU.

VECTOR GENE

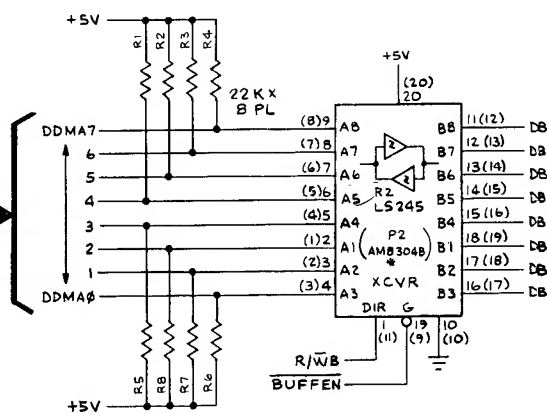
VECTOR G



GENERATOR RAM

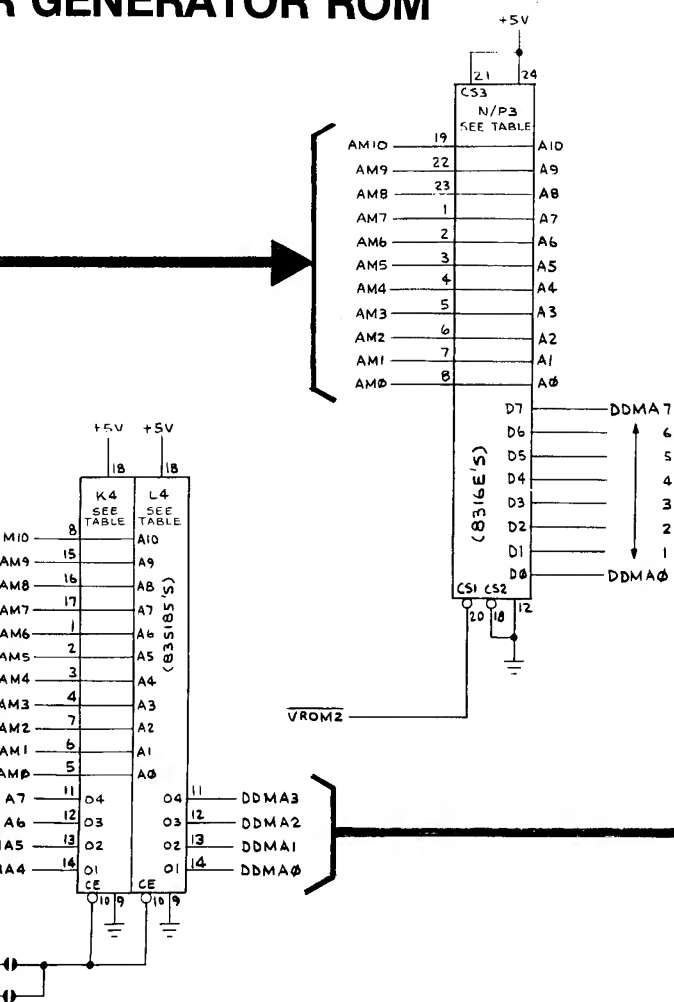


VECTOR GENERATOR DATA BUFFER



* USE PIN NUMBERS IN PARENTHESES IF BOARD CONTAINS AM83048 INSTEAD OF 74LS245

R GENERATOR ROM



VECTOR MEMORY ROM/PROM SUBSTITUTION				SPLIT PAD TO BE BRIDGED AT K/L3
ROM #	LOC	PROM #	LOC	
035127	N/P3	035129	K4	
	R3	035130	L4	
			K4	
			L4	

The vector generator memory consists of RAM and 4K of ROM. It may be directly accessed by the MPU of the microcomputer through the direct memory access processor (DMA). Data is written in from the microcomputer thru data buffer R2 when BUFFER R/WB are low.

The 2Kx8 vector generator program memory chip N/P3 may be substituted two equivalent 1Kx8 chips in location K4 L4.

TO/FROM
MPU DATA BUS
SHEET 1, SIDE B,

B8	11(12)	DB7
B7	12(13)	DB6
B6	13(14)	DB5
B5	14(15)	DB4
B4	15(16)	DB3
B1	18(19)	DB2
B2	17(18)	DB1
B3	16(17)	DB0
10	(10)	

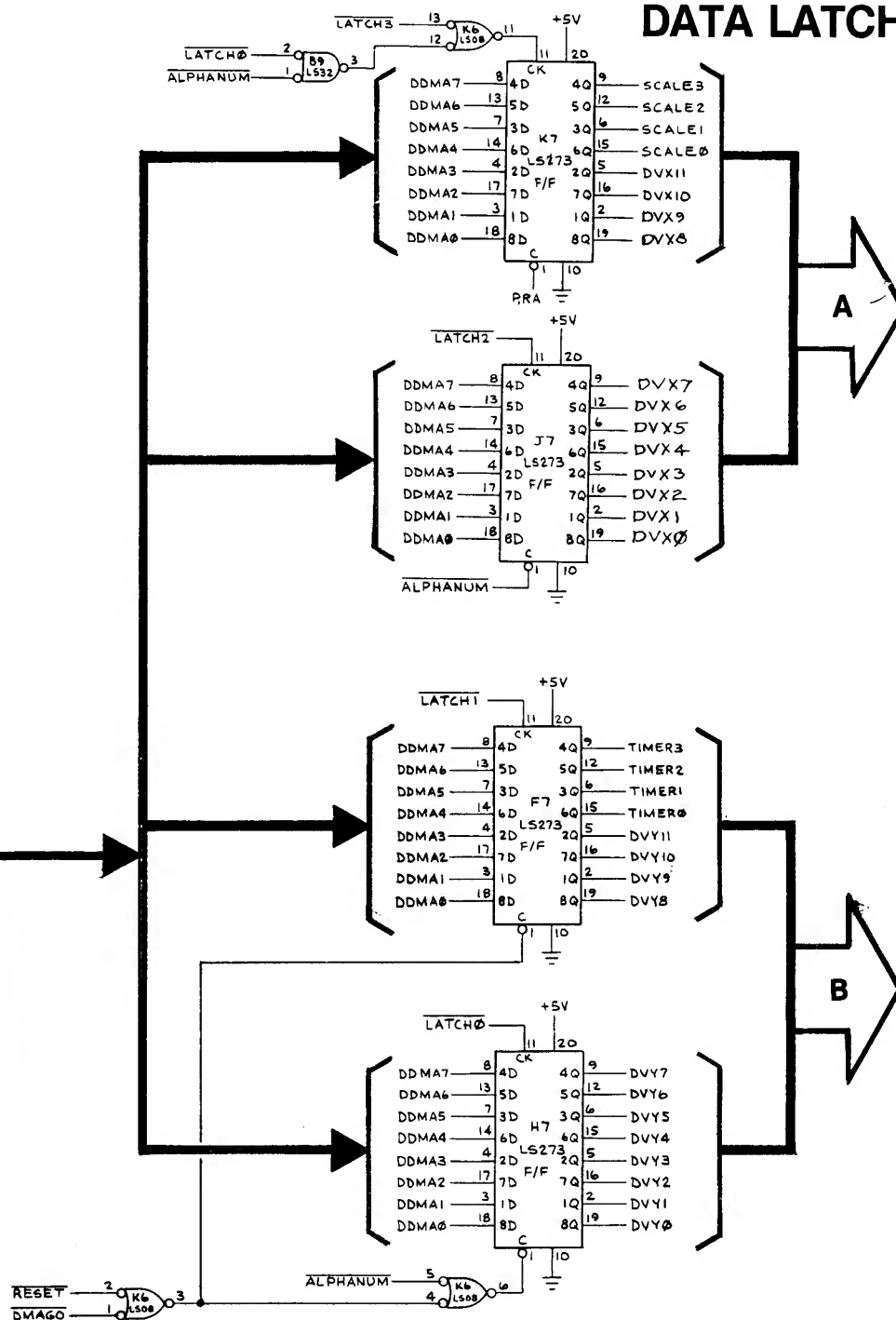
IS IN PAREN-
CONTAINS
OF 74LS245

SPLIT PAD TO BE BRIDGED AT K/L3	
LOC	
K4	
L4	
K4	
L4	

y consists of 2K
y be directly ac-
microcomputer
access process
the microcom-
n **BUFFEN** and

erator program
ubstituted with
location K4 and

VECTOR GENERATOR MEMORY DATA LATCHES



The data latches consist of latch 0 (H7), latch 1 (F7), latch 2 (J7), and latch 3 (K7). Inputs DDMA0 thru DDMA7 are the data outputs from the vector generator memory.

Latches 0 thru 2 are directly clocked by the rising edge of the LATCH0, LATCH1, and LATCH2 outputs from the vector generator's state machine. Latch 3 is clocked by LATCH3 or by LATCH0, if ALPHANUM is low. Latch 0 is cleared when RESET, DMAGO, or ALPHANUM goes low. Latch 1 is cleared by ALPHANUM.